

NCE 60V Complementary MOSFET

Description

The NCE603S uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

N channel

- $V_{DS} = 60V, I_D = 6A$
 $R_{DS(ON)} < 60m\Omega @ V_{GS} = 10V$

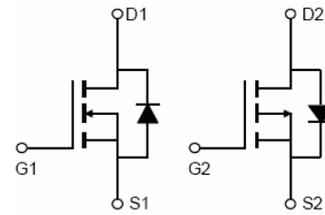
p channel

- $V_{DS} = -60V, I_D = -6A$
 $R_{DS(ON)} < 80m\Omega @ V_{GS} = -10V$

- High density cell design for ultra low R_{dson}
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

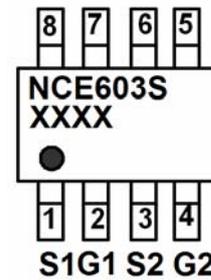
Application

- H-bridge
- Inverters

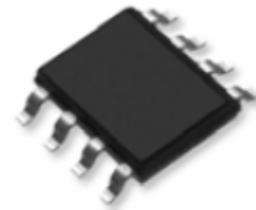


Schematic diagram

D1 D1 D2 D2



Marking and pin assignment



SOP-8 top view

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCE603S	NCE603S	SOP-8	Ø330mm	12mm	2500 units

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	N-Channel	P-Channel	Unit	
Drain-Source Voltage	V_{DS}	60	-60	V	
Gate-Source Voltage	V_{GS}	± 20	± 20	V	
Continuous Drain Current	I_D	$T_C = 25^\circ C$	6	-6	A
		$T_C = 100^\circ C$	4.2	-4.2	
Pulsed Drain Current ^(Note 1)	I_{DM}	30	-30	A	
Maximum Power Dissipation	P_D	2	2	W	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 175	-55 To 175	$^\circ C$	

Thermal Characteristic

N-channel	Thermal Resistance, Junction-to- Ambient ^(Note 2)	$R_{\theta JA}$	75	$^\circ C/W$
P-channel	Thermal Resistance, Junction-to- Ambient ^(Note 2)	$R_{\theta JA}$	50	$^\circ C/W$

N-Channel Electrical Characteristics (T_A=25°C unless otherwise noted)

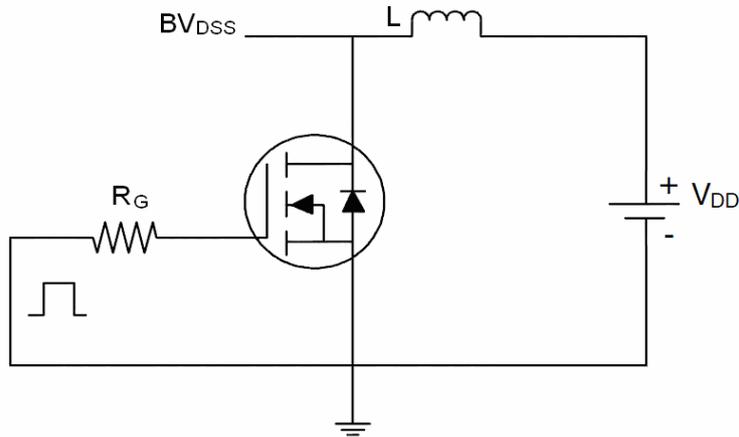
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1.0	2.0	3.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =6A	-	37	44	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =6A	11	-	-	S
Dynamic Characteristics (Note 4)						
Input Capacitance	C _{ISS}	V _{DS} =30V, V _{GS} =0V, F=1.0MHz	-	450	-	PF
Output Capacitance	C _{OSS}		-	61	-	PF
Reverse Transfer Capacitance	C _{rss}		-	27	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =30V, R _L =2.5Ω V _{GS} =10V, R _G =3Ω	-	4.2	-	nS
Turn-on Rise Time	t _r		-	3.4	-	nS
Turn-Off Delay Time	t _{d(off)}		-	16	-	nS
Turn-Off Fall Time	t _f		-	2	-	nS
Total Gate Charge	Q _g	V _{DS} =30V, I _D =6A, V _{GS} =10V	-	10	-	nC
Gate-Source Charge	Q _{gs}		-	2.4	-	nC
Gate-Drain Charge	Q _{gd}		-	3.6	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _S =6A	-	-	1.2	V
Diode Forward Current	I _S		-	-	6	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F =6A di/dt = 100A/μs (Note3)	-	27	-	nS
Reverse Recovery Charge	Q _{rr}		-	30	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

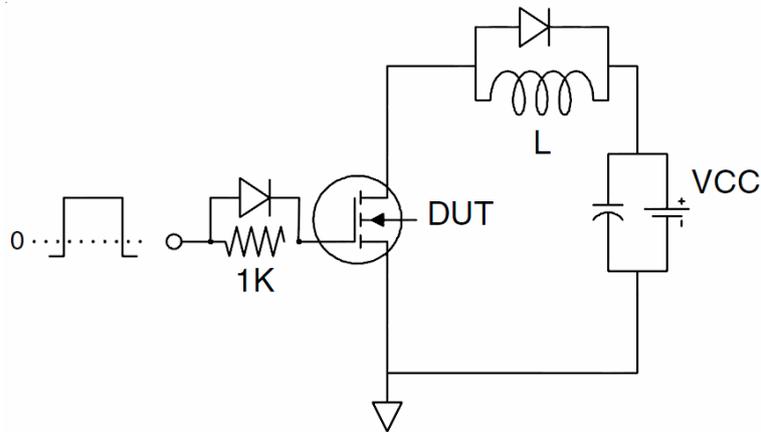
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

Test Circuit

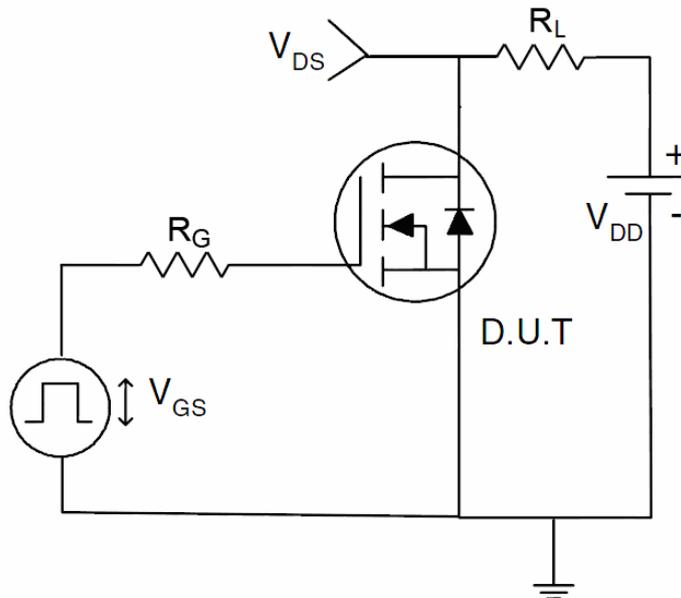
1) E_{AS} test Circuit



2) Gate charge test Circuit



3) Switch Time Test Circuit



N-Channel Typical Electrical and Thermal Characteristics (Curves)

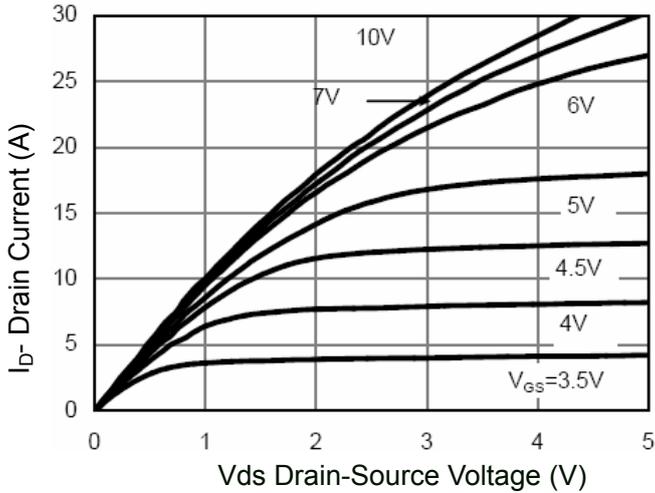


Figure 1 Output Characteristics

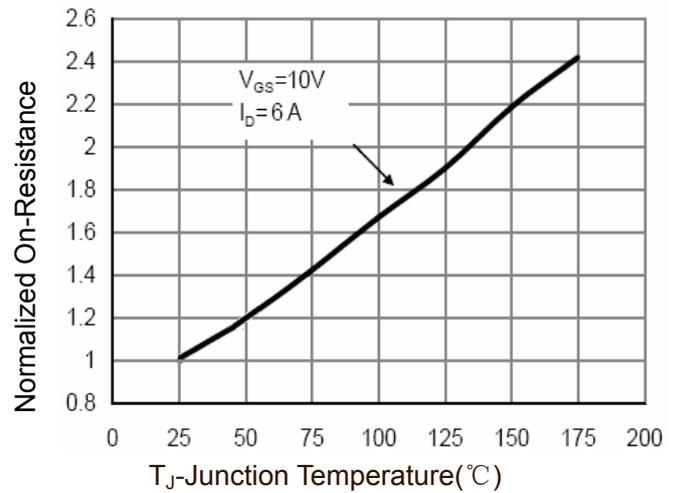


Figure 4 R_{dson} -Junction Temperature

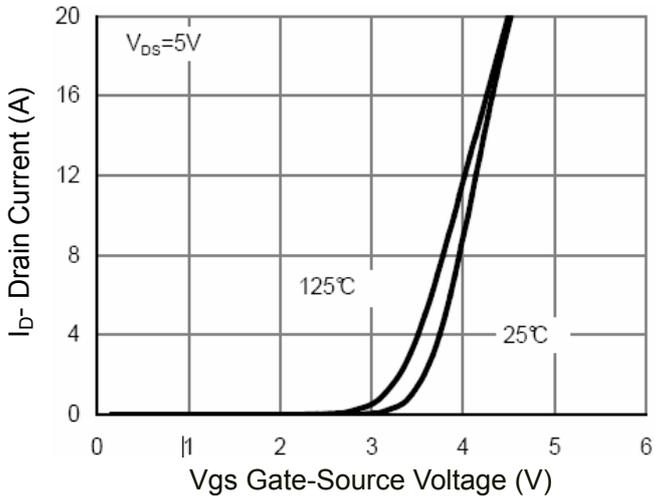


Figure 2 Transfer Characteristics

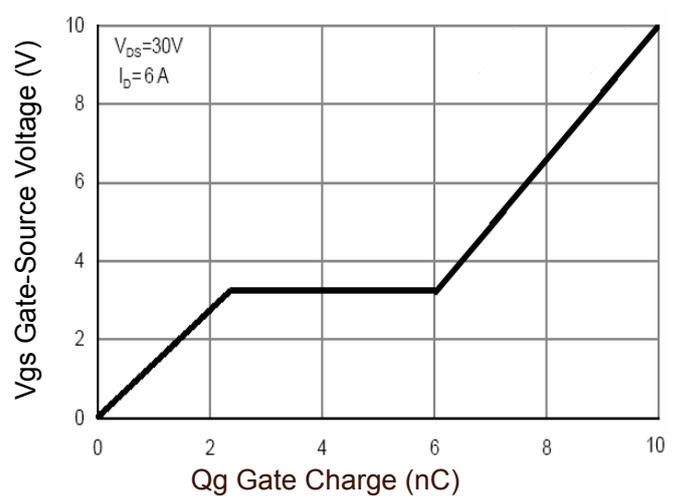


Figure 5 Gate Charge

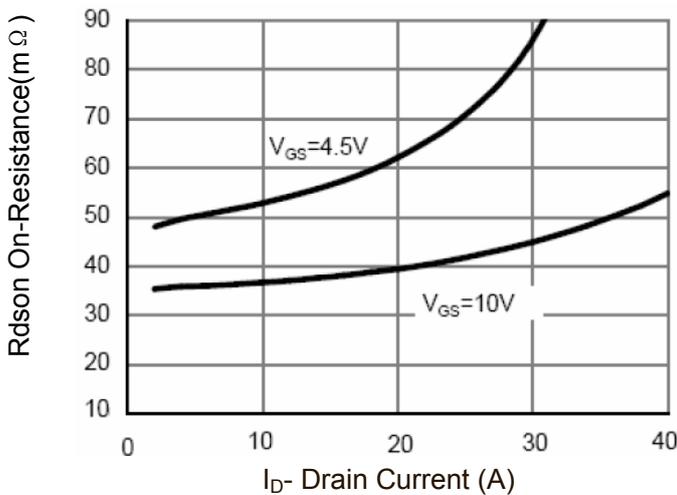


Figure 3 R_{dson} - Drain Current

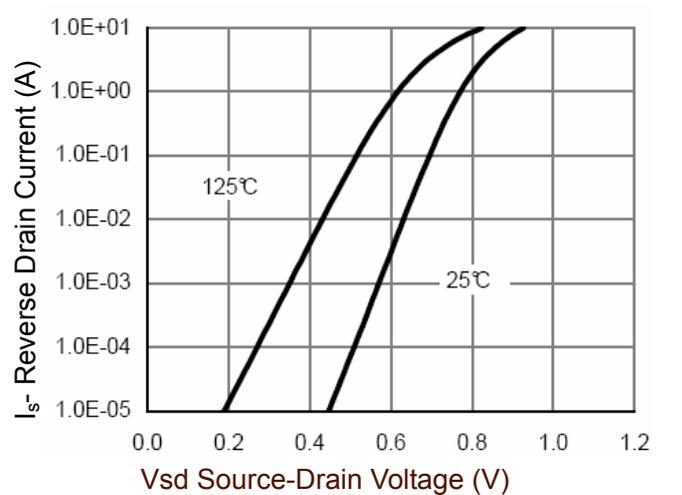


Figure 6 Source- Drain Diode Forward

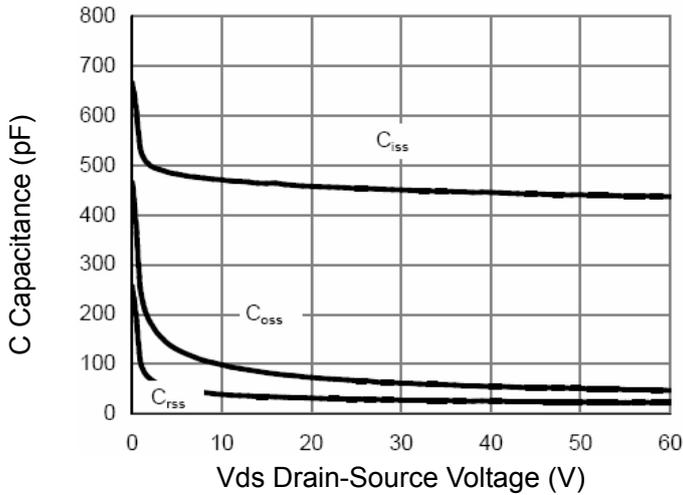


Figure 7 Capacitance vs Vds

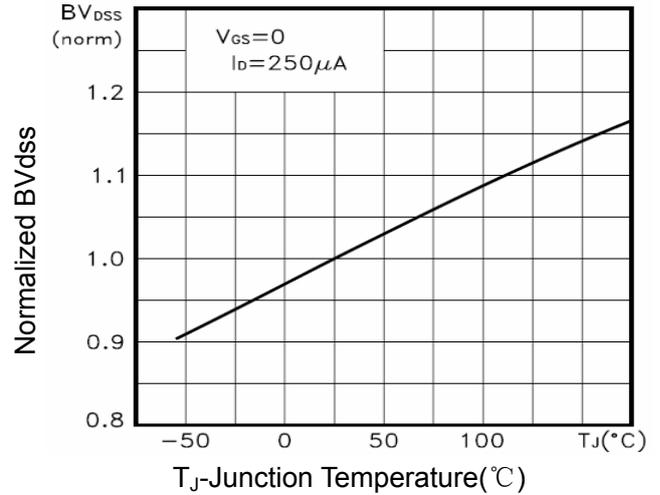


Figure 9 BV_{DSS} vs Junction Temperature

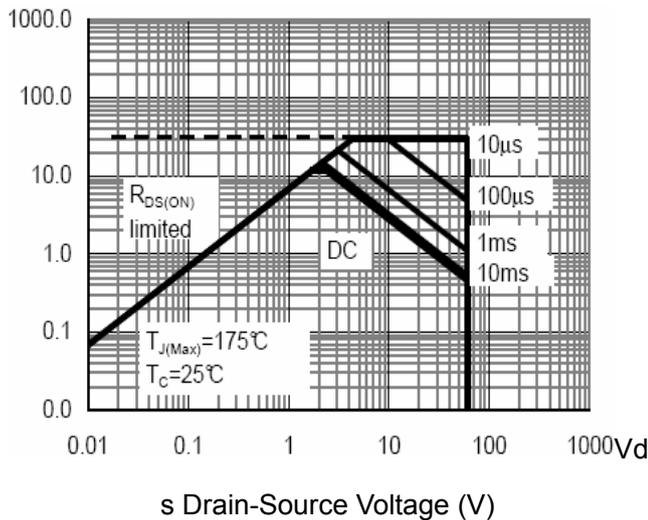


Figure 8 Safe Operation Area

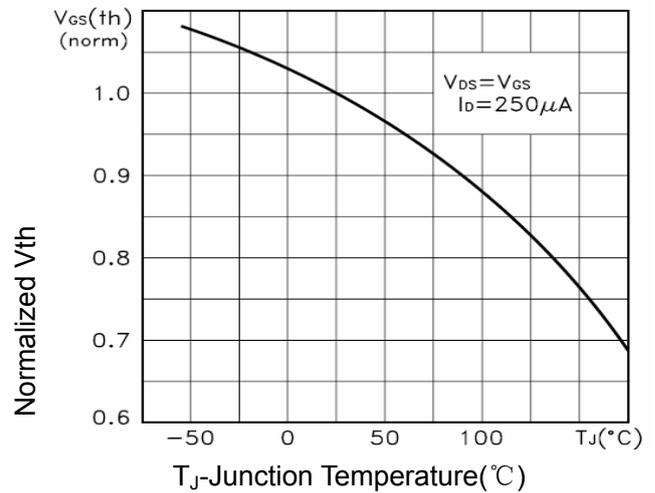


Figure 10 $V_{GS(th)}$ vs Junction Temperature

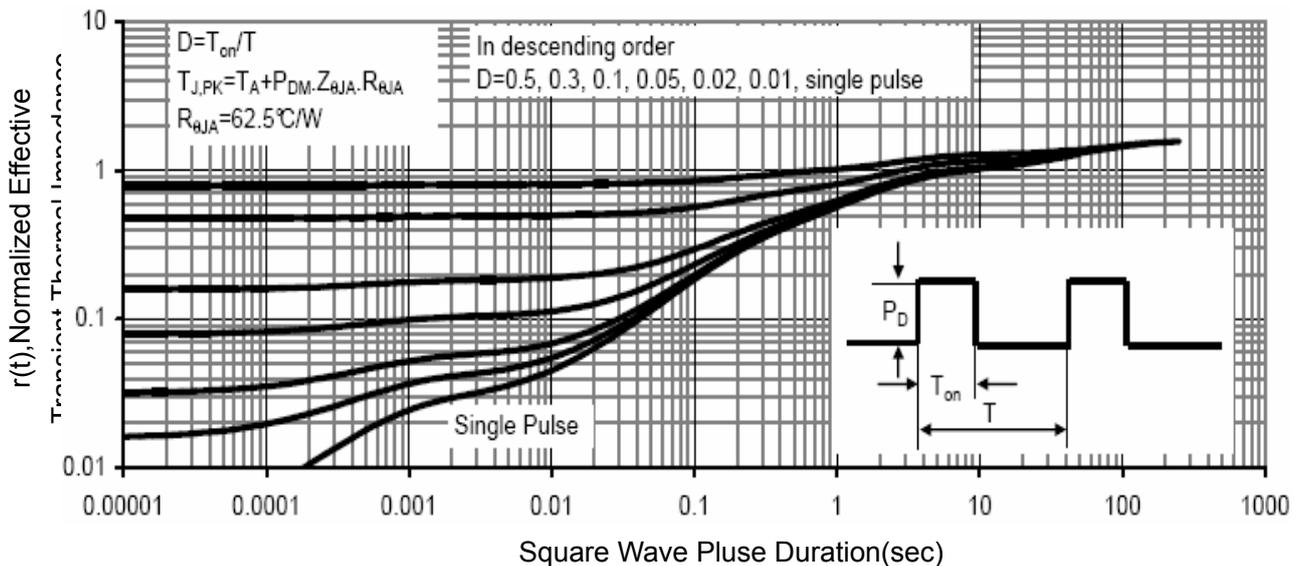


Figure 11 Normalized Maximum Transient Thermal Impedance

P-Channel Electrical Characteristics (T_C=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250μA	-60	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-60V, V _{GS} =0V	-	-	-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1.5	-2.6	-3.0	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-6A	-	64	80	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-5V, I _D =-6A	11	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =-30V, V _{GS} =0V, F=1.0MHz	-	960	-	PF
Output Capacitance	C _{oss}		-	86	-	PF
Reverse Transfer Capacitance	C _{rss}		-	38	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-30V, R _L =2.5Ω V _{GS} =-10V, R _G =3Ω	-	9	-	nS
Turn-on Rise Time	t _r		-	10	-	nS
Turn-Off Delay Time	t _{d(off)}		-	25	-	nS
Turn-Off Fall Time	t _f		-	11	-	nS
Total Gate Charge	Q _g	V _{DS} =-30V, I _D =-6A, V _{GS} =10V	-	15.8	-	nC
Gate-Source Charge	Q _{gs}		-	3	-	nC
Gate-Drain Charge	Q _{gd}		-	3.5	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =-6A	-	-	-1.2	V
Diode Forward Current (Note 2)	I _S		-	-	-6	A
Reverse Recovery Time	t _{rr}	T _J = 25°C, I _F = -6A di/dt = 100A/μs (Note3)	-	27.5	-	nS
Reverse Recovery Charge	Q _{rr}		-	30	-	nC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

P-Channel Typical Electrical and Thermal Characteristics (Curves)

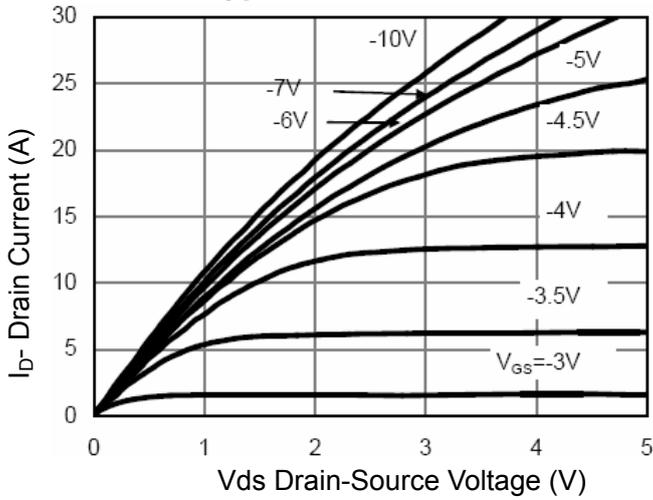


Figure 1 Output Characteristics

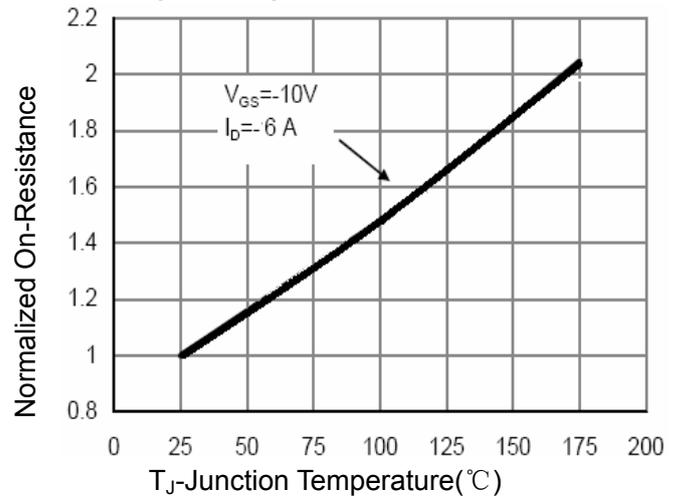


Figure 4 R_{dson} -Junction Temperature

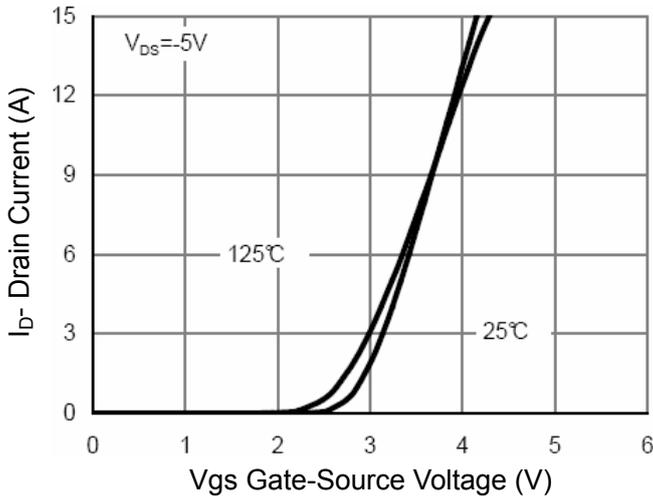


Figure 2 Transfer Characteristics

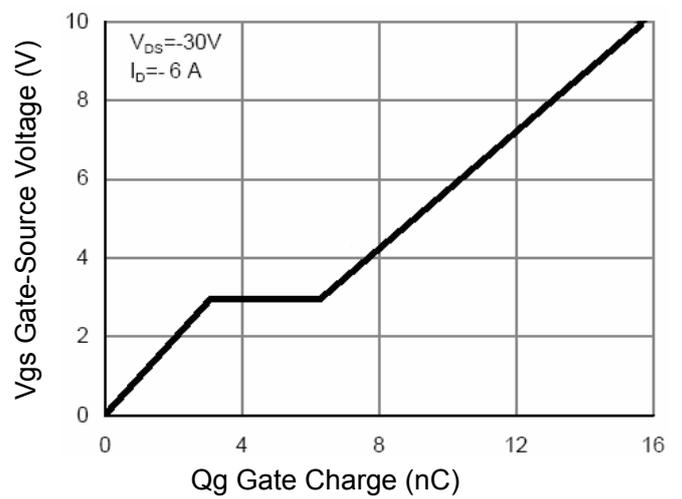


Figure 5 Gate Charge

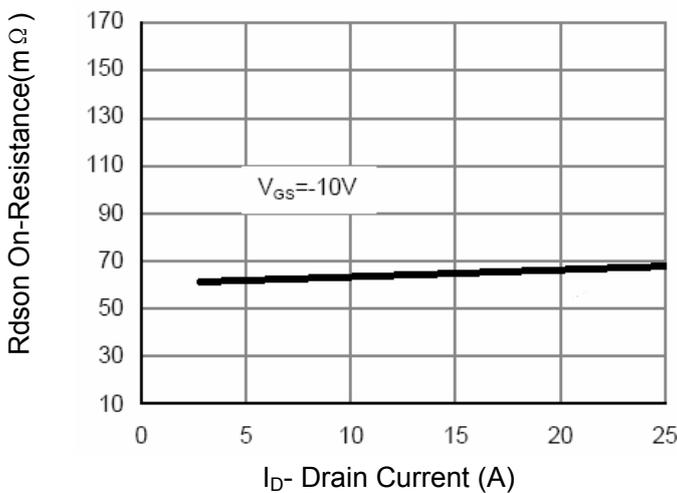


Figure 3 R_{dson} - Drain Current

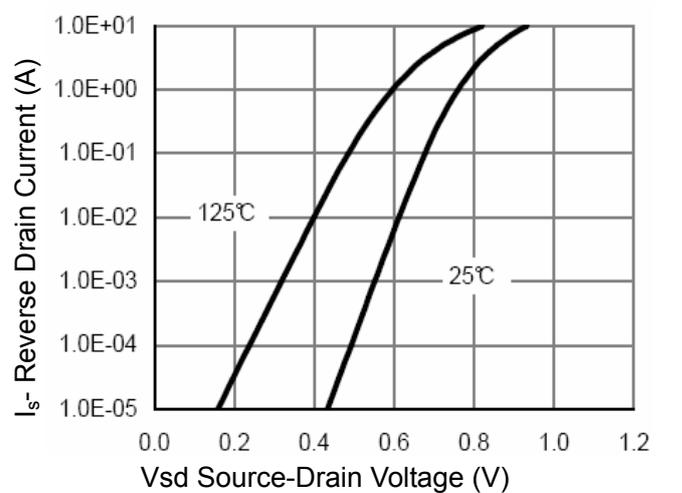


Figure 6 Source- Drain Diode Forward

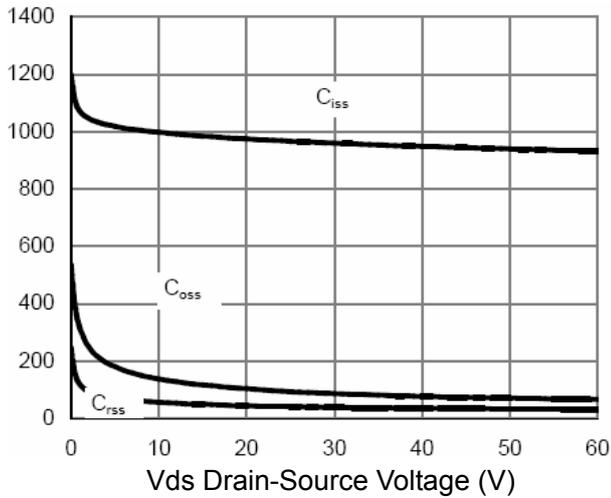


Figure 7 Capacitance vs Vds

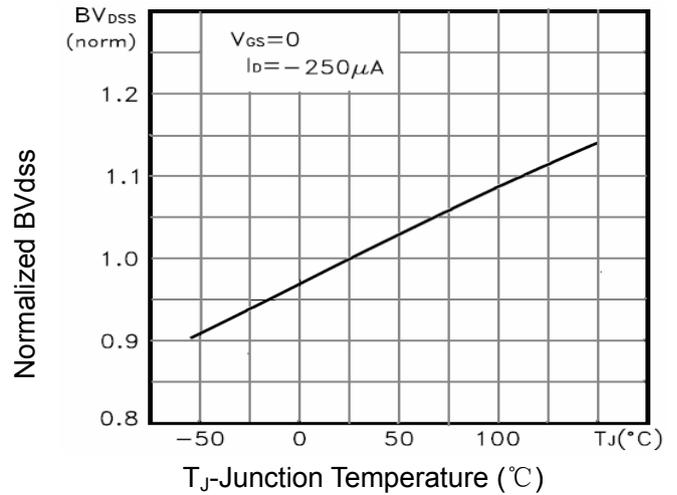


Figure 9 BV_{DSS} vs Junction Temperature

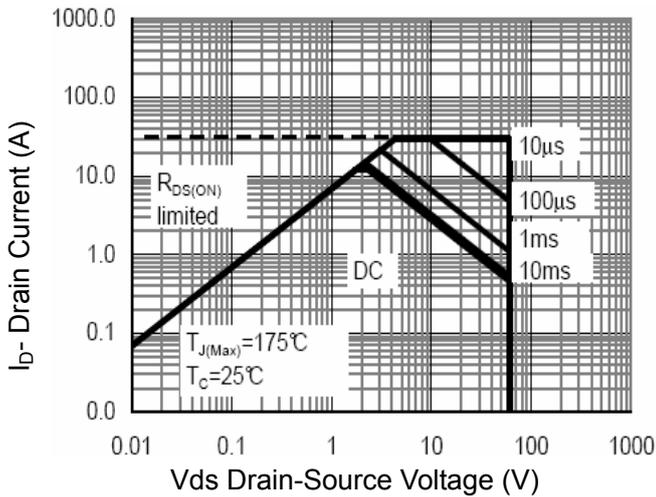


Figure 8 Safe Operation Area

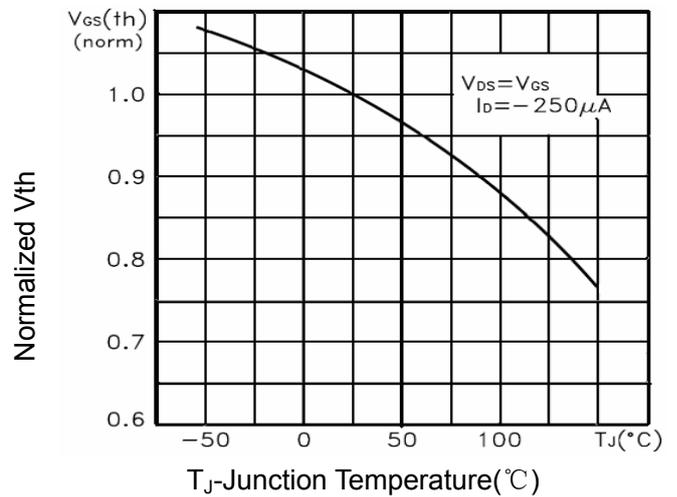


Figure 10 $V_{GS(th)}$ vs Junction Temperature

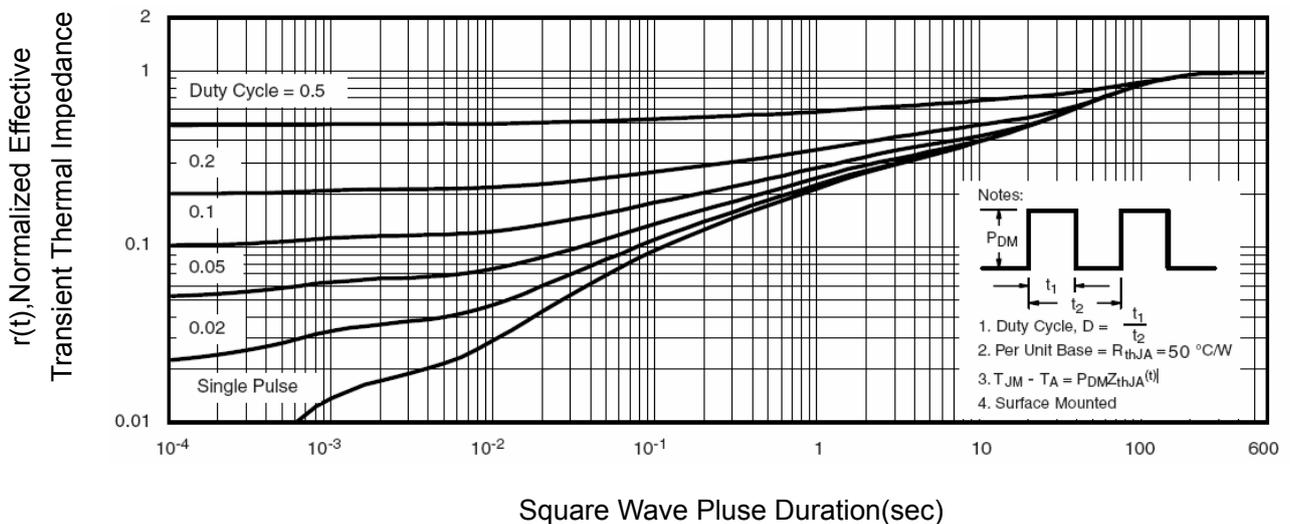
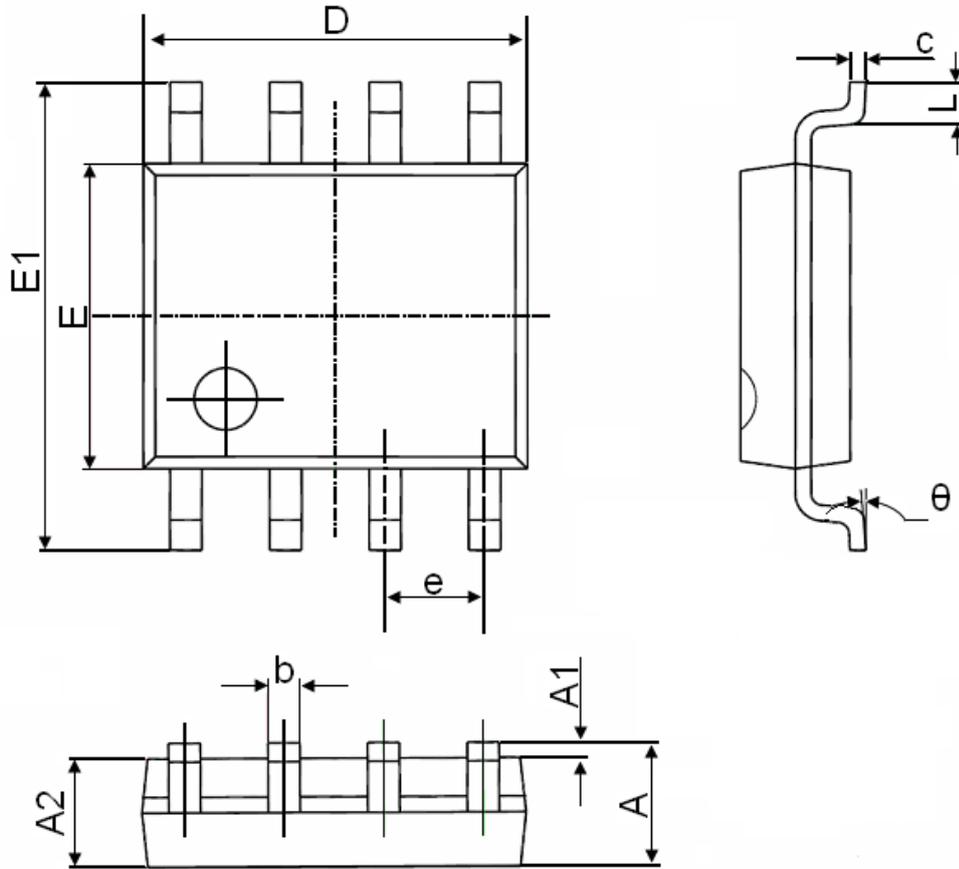


Figure 11 Normalized Maximum Transient Thermal Impedance

SOP-8 Package Information


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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