# NCE1512IA

### NCE N-Channel Enhancement Mode Power MOSFET

### **Description**

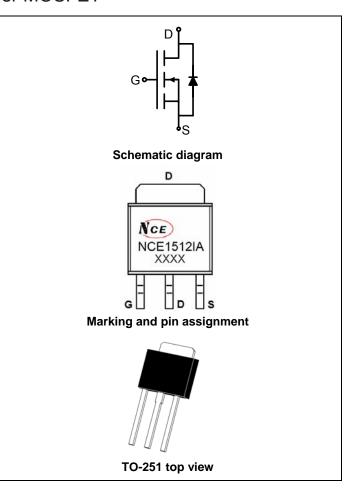
The NCE1512IA uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

#### **General Features**

- $V_{DS}$  = 150V, $I_{D}$  =12A  $R_{DS(ON)}$  <160mΩ @  $V_{GS}$ =10V (Typ:130mΩ)
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

## **Application**

- Power switching application
- Hard switched and high frequency circuits



#### **Package Marking and Ordering Information**

<b>Device Marking</b>	Device	Device Package	Reel Size	Tape width	Quantity
NCE1512IA	NCE1512IA	TO-251	-	-	-

## Absolute Maximum Ratings (T<sub>C</sub>=25 ℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	150	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Drain Current-Continuous	I <sub>D</sub>	12	Α
Drain Current-Pulsed (Note 1)	I <sub>DM</sub>	50	Α
Maximum Power Dissipation	P <sub>D</sub>	55	W
Operating Junction and Storage Temperature Range	$T_{J}$ , $T_{STG}$	-55 To 175	$^{\circ}$ C

#### **Thermal Characteristic**

Thermal Resistance, Junction-to-Case (Note 2)	R <sub>0</sub> JC	2.7	°C/W	
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# http://www.ncepower.com

# NCE1512IA

# Electrical Characteristics (T<sub>C</sub>=25 <sup>°</sup>C unless otherwise noted)

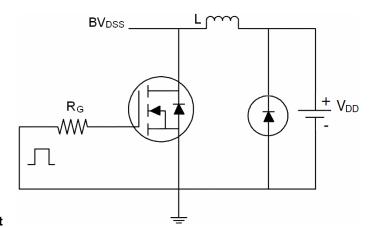
Parameter	Symbol	Condition	Min	Тур	Max	Unit	
Off Characteristics							
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V I <sub>D</sub> =250μA	150	-	-	V	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =150V,V <sub>GS</sub> =0V	-	-	1	μA	
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V,V <sub>DS</sub> =0V	-	-	±100	nA	
On Characteristics (Note 3)							
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> ,I <sub>D</sub> =250μA	1.5	2	2.5	V	
Drain-Source On-State Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =5A	-	130	160	mΩ	
Forward Transconductance	<b>g</b> FS	V <sub>DS</sub> =15V,I <sub>D</sub> =10A	-	15	-	S	
Dynamic Characteristics (Note4)							
Input Capacitance	C <sub>lss</sub>	)/ OF)/)/ O)/	-	900	-	PF	
Output Capacitance	C <sub>oss</sub>	$V_{DS}$ =25V, $V_{GS}$ =0V, F=1.0MHz	-	115	-	PF	
Reverse Transfer Capacitance	C <sub>rss</sub>	F=1.UIVITZ	-	70	-	PF	
Switching Characteristics (Note 4)							
Turn-on Delay Time	t <sub>d(on)</sub>		-	8	-	nS	
Turn-on Rise Time	t <sub>r</sub>	$V_{DD}$ =75 $V$ , $I_D$ =1 $A$ , $R_L$ =75 $\Omega$	-	10	-	nS	
Turn-Off Delay Time	t <sub>d(off)</sub>	$V_{GS}$ =10 $V$ , $R_{G}$ =6 $\Omega$	-	20	-	nS	
Turn-Off Fall Time	t <sub>f</sub>	1	-	15	-	nS	
Total Gate Charge	Qg	\/ -75\/  -4.50	-	19		nC	
Gate-Source Charge	Q <sub>gs</sub>	V <sub>DS</sub> =75V,I <sub>D</sub> =1.5A,	-	5.5	-	nC	
Gate-Drain Charge	Q <sub>gd</sub>	- V <sub>GS</sub> =10V	-	7	-	nC	
Drain-Source Diode Characteristics						•	
Diode Forward Voltage (Note 3)	V <sub>SD</sub>	V <sub>GS</sub> =0V,I <sub>S</sub> =2A	-	-	1.2	V	
Diode Forward Current (Note 2)	Is		-	-	12	Α	

#### Notes:

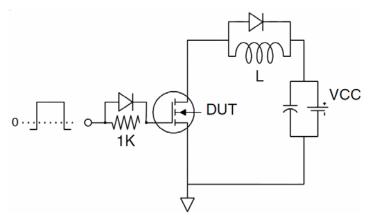
- 1. Repetitive Rating: Pulse width limited by maximum junction temperature.
- 2. Surface Mounted on FR4 Board, t ≤ 10 sec.
- **3.** Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.
- 4. Guaranteed by design, not subject to product

# **Test Circuit**

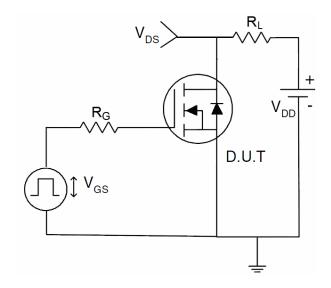
# 1) E<sub>AS</sub> Test Circuit



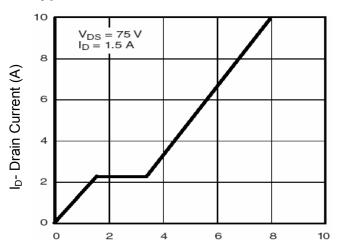
## 2) Gate Charge Test Circuit



## 3) Switch Time Test Circuit

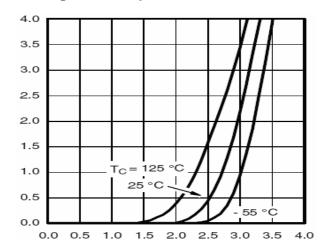


# **Typical Electrical and Thermal Characteristics (Curves)**



Vds Drain-Source Voltage (V)





ID- Drain Current (A)

Vgs Gate-Source Voltage (V)

# **Figure 2 Transfer Characteristics**

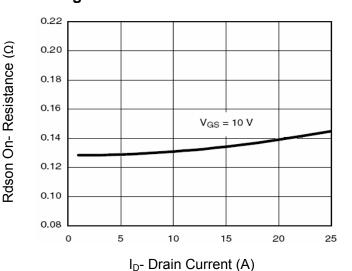
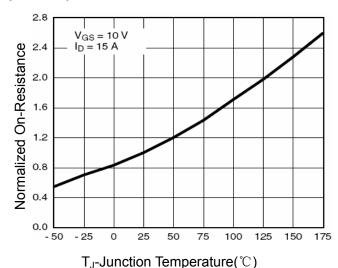


Figure 3 Rdson- Drain Current



**Figure 4 Rdson- Junction Temperature** 

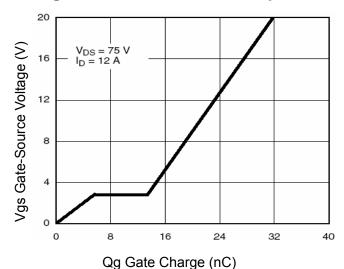
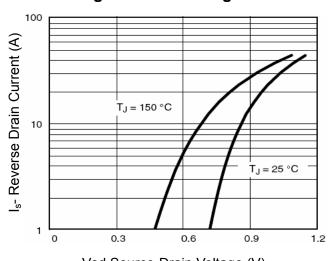


Figure 5 Gate Charge



Vsd Source-Drain Voltage (V)

Figure 6 Source- Drain Diode Forward

150

100

125

 $I_D = 250 \, \mu A$ 

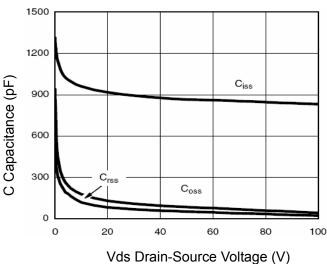
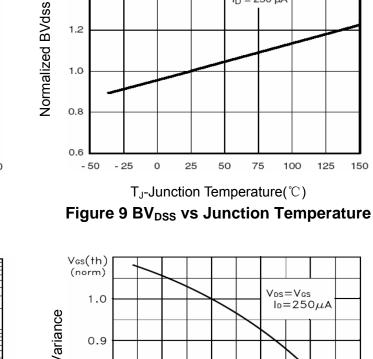


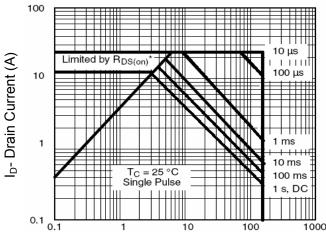
Figure 7 Capacitance vs Vds



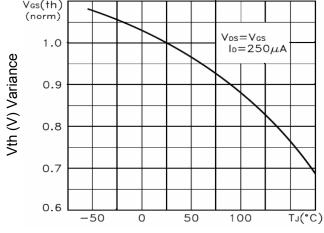
1.6

1.4

1.2



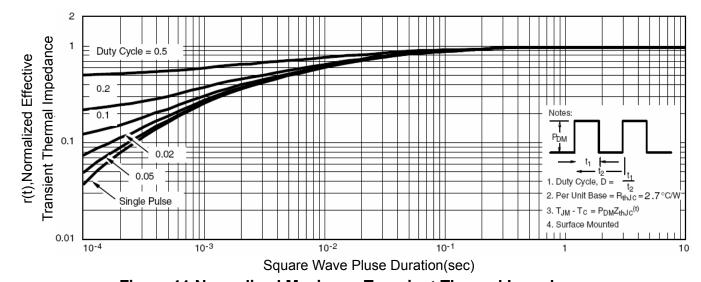
Vds Drain-Source Voltage (V) Figure 8 Safe Operation Area



50

 $T_J$ -Junction Temperature( $^{\circ}$ C)

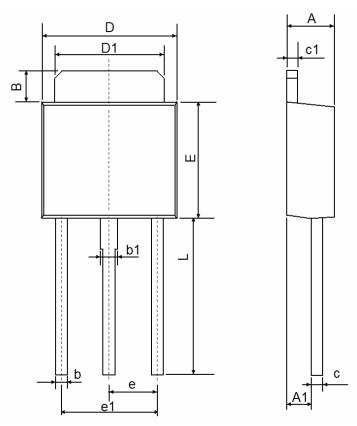
Figure 10 V<sub>GS(th)</sub> vs Junction Temperature



**Figure 11 Normalized Maximum Transient Thermal Impedance** 



# **TO-251 Package Information**



Cumah al	Dimensions I	n Millimeters	Dimensions In Inches		
Symbol	Min.	Max.	Min.	Max.	
А	2.200	2.400	0.087	0.094	
A1	1.050	1.350	0.042	0.054	
В	1.350	1.650	0.053	0.065	
b	0.500	0.700	0.020	0.028	
b1	0.700	0.900	0.028	0.035	
С	0.430	0.580	0.017	0.023	
c1	0.430	0.580	0.017	0.023	
D	6.350	6.650	0.250	0.262	
D1	5.200	5.400	0.205	0.213	
Е	5.400	5.700	0.213	0.224	
е	2.300 TYP		0.091 TYP		
e1	4.500	4.700	0.177	0.185	
L	7.500	7.900	0.295	0.311	

#### **Notes**

- 1. All dimensions are in millimeters.
- 2. Tolerance ±0.10mm (4 mil) unless otherwise specified
- 3. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
- 4. Dimension L is measured in gauge plane.
- $5. \ Controlling \ dimension \ is \ millimeter, \ converted \ inch \ dimensions \ are \ not \ necessarily \ exact.$

**Pb-Free Product** 

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